FPGA Implementation of Sequential Logic

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EECS: 1100 Digital Logic Design
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Lab Assignment #12

1. Objectives

- introduction to programming techniques of CPLDs and FPGAs,
- gaining experience in working with CPLDs and FPGAs,
- learning the simulation process using EDA tools,
- gaining a close insight into the functioning and properties of synchronous counters,
- developing skills in the composition and testing of sequential logic circuits.

2. Prelab Assignment

The work on two designs (projects) of Lab Assignment #11 has produced:

- logic designs of a down-counting BCD counter, and an up-counting modulo-6 counter using negative edge triggered JK-flip-flops,
- the down_bcd.gdf, and up_mod6.gdf graphic design files containing the logic circuit diagrams of the designed counters, as created by the Altera's Schematic Capture tool.

These will be used as the starting point of the current assignment to cut down on the time needed for its completion. Further processing will require using other Altera's Electronic Design Automation (EDA) tools whose descriptions and tutorials are available for downloading from the Altera's web site:

http://www.altera.com/html/literature/lsig.html

which you have already visited in Lab Assignment #2. Once there, select the link

° Section 3: MAX+PLUS II Tutorial

to open the document which contains information pertinent to the current assignment.

Hint1: The document is in .pdf format, so Acrobat Reader will open the document for you. In Acrobat Reader's *Print* window you might need to request page numbers which are by 154 less than page numbers shown in the document because Acrobat Reader does not see the shown page numbering, but sees instead the actual pages present in the document. See Lab Assignment #2 for more details.

2.1 COMPILING THE PROJECTS

The Session 6: Compile the project is to be found on pages numbered 216 through 228 of the opened Altera's tutorial document.

Hint#2 The tutorial assumes at that point that after the completion of the schematic entry, and while the schematic editor window was still showing a counter's logic circuit, the following actions have been completed without any errors or warnings having been reported:

a. selecting from the MAX+PLUS II window: File_Save,
b. selecting from the MAX+PLUS II window: File_Project_Set Project to Current File,
c. selecting from the MAX+PLUS II window: File_Project_Save&Check,
d. selecting from the MAX+PLUS II window: File_Project_Save&Compile.

If in doubt as to what has been done in your case, repeating these actions is necessary.

2.1.1 Follow the tutorial to compile your two counter projects. The major steps to be executed (in the order given below) include:

- have the MAX+PLUS II application running,
- open the Compiler from the MAX+PLUS II window by selecting:

  MAX+PLUS II→Compile,
- set the device type to match the one on the protoboard by selecting: **Assign→Device**, which displays the Device dialog box where the following steps ought to be performed,
- set the **Device Family** to: MAX7000S,
- make sure that the *Show Only Fastest Speed Grades* check box is **not** checked,
- select in the **Devices** scroll window: EPM7128SLC84-7,
- click the OK button;
- select: **Assign→Global Project Logic Synthesis**, which displays the Global Project Logic Synthesis dialog box where,
- in the section **MAX Device Synthesis Options** have checked the box **Multi-Level Synthesis for MAX5000/7000 Devices**,
- in the section **Automatic Global** uncheck all check boxes but the box **Clear** which should remain checked,
- click the OK button;

Hint#3 This last action has left the global CLR signal hardwired to the pin #1 (See Figure A.4-1); CLR, therefore, does not appear in Table TA.2-1.

- select: **Assign→Pin/Location/Chip** to assign the pin numbers to I/O signals of your logic circuit according to Table TA.2-1,

Table TA.2-1 Signal to pin assignment

Signal	Q_D	Q_C	Q_B	Q_A	Count	PRE
Pin #	12	15	17	18	24	30

in the displayed Pin/Location/Chip dialog box, click on the **Search** button, to open the next dialog box where,

- click on the **List** button, which displays a list of signal names from Table TA.2-1,
- select, by clicking on it, one of the signal names,
- click the OK button to close the dialog box;
- back in the Pin/Location/Chip dialog box, use the **Pin** scroll window to select the corresponding pin number from Table TA.2-1,
- click on the ADD button;
- repeat the signal/pin# couple assignment for the rest of the signals from Table TA.2-1;
- close the Pin/Location/Chip dialog box;

Hint#4 The BCD counter does, and the modulo-6 counter does not have the signal Q_D .

- from MAX+PLUS II window select: **File**→**Project**→**Save&Compile**, which will display the compiler widow and start the checking process,
- in case that no errors were reported by the checker, click on the **Start** button, which will run the compiler.

Hint#5 All errors reported after any of the above listed actions must be removed before proceeding to the next action.

2.2 CREATING THE STIMULUS FOR SIMULATION

Successful simulation of a designed logic circuit demonstrates that the designer has prepared a correct logic design and circuit. There are other reasons for which your implementation may fail to function correctly than an incorrect design. One, therefore, wants to make sure before testing the implementation that an erroneous design is not being tested.
To create the *Simulator Channel Files* for your counter circuits, follow the Session 9 of the tutorial, on pages number 246 through 254 of the Altera's tutorial.

2.3 SIMULATING THE COUNTER CIRCUITS

To invoke the simulation tool and perform the simulation of your counter circuits, follow the Session 10 of the Altera's tutorial, pages number 256 through 259.

3. Lab Equipment and Circuit Components

3.1 EQUIPMENT

Equipment to be used includes:

- Altera protoboard UP-1,
- Agilent E3631A DC power supply (12V),
- Function generator: Agilent 33120A,
- Mixed-Signal oscilloscope Agilent 54645D,
- Dell GxaEM computer system.

3.2 LOGIC GATE AND CIRCUIT COMPONENTS

- Altera MAX series FPGA EPM7128SLC84-7 (1)

4. Lab Assignment

4.1 GENERAL CONNECTIONS TO THE UP-1 PROTOBOARD

Prior to programming any designed circuits into the Altera EPM7128SLC84-7 FPGA on the protoboard UP-1, the following two connections must be established.

4.1.1 Have the Altera UP-1 protoboard connected to the parallel port of the Dell GxaEM computer through the ByteBlaster Parallel Port Download Cable.

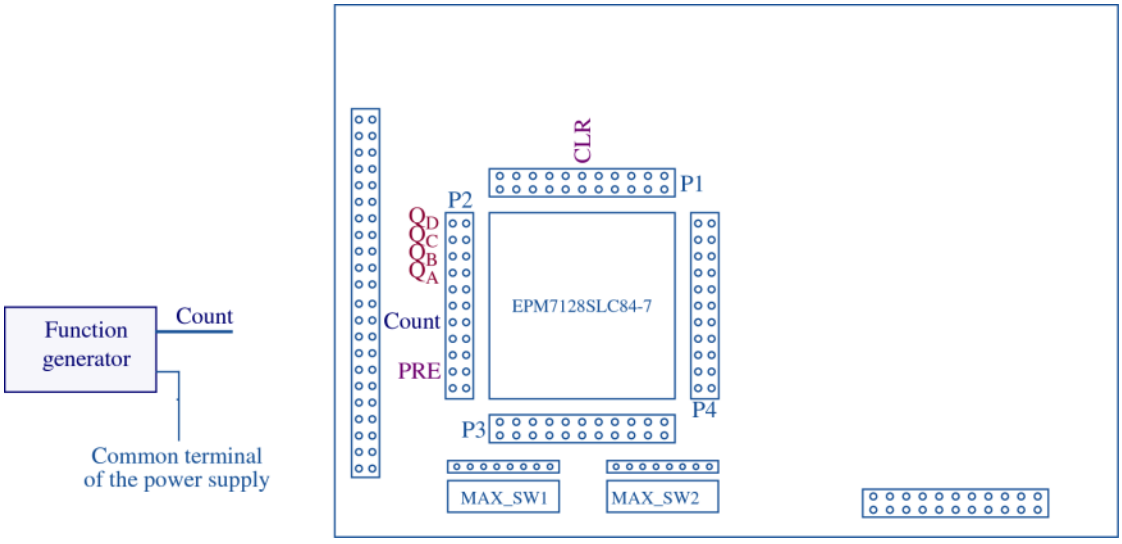

Figure A.4-1 Partial view of the Altera's UP-1 protoboard showing the programmed signal pin locations.

4.1.2 Have the Altera UP-1 protoboard's +/- RAW power terminals connected to the +12V/COMMON power supply outlets (red/black), and powered up.

4.2 EXPERIMENT WITH THE DOWN-COUNTING BCD COUNTER

4.2.1 Follow the Session 13 of the tutorial, pages number 273 through 275, to invoke the Programmer tool, and execute the programming of the EPM7128SLC84-7 FPGA device to perform the function of your counter circuit. Apply your bcd_down design/project. Proceed to the rest of the experiment after the Programmer tool has reported a successful downloading of the down_bcd.pof file to the FPGA device.

4.2.2 Make the following connections to the Altera UP-1 protoboard:

- output of the function generator: to the pin # 24 of the EPM7128SLC84-7 device,
- switch MAX_SW1-1: to the pin # 30 of the EPM7128SLC84-7 device,
- switch MAX_SW1-2: to the pin # 1 of the EPM7128SLC84-7 device.

Turn on the switches MAX_SW1-1 through MAX_SW1-2 (upper position).

4.2.3 Connect the digital channels D0 through D4 of the Mixed-Signal oscilloscope Agilent 54645D to the pins of the EPM7128SLC84-7 on the Altera protoboard:

- digital channel D0: to the pin # 18 of the EPM7128SLC84-7 device,
- digital channel D1: to the pin # 17 of the EPM7128SLC84-7 device,
- digital channel D2: to the pin # 15 of the EPM7128SLC84-7 device,
- digital channel D3: to the pin # 12 of the EPM7128SLC84-7 device,
- digital channel D4 to the pin # 24 of the EPM7128SLC84-7 device.

Establish a ground connection. Turn on digital channels D0 through D4, and rename the channels D0 through D4 as, Q_A, Q_B, Q_C, Q_D, and CNT respectively.

4.2.4 Adjust the frequency of the Agilent 33120A function generator to 1.25 MHz. Set the triggering mode of the Agilent 54645D to the combination 1001 on channels D0 through D3. Hit the key *Single* on the Agilent 54645D. Adjust the display so that the combination 1001 of the counter's output signals is positioned at the left side of the screen, and that the whole screen shows ten percent more than two periods of the signal at Q_D.

4.2.5 Observe the captured BCD down-counter's output waveforms. Compare these waveforms with the contents of Table T2.1-1 of the Assignment #11 Report.

4.2.6 Save the Screen Image of the correct waveforms of channels D0 through D4 to a file named l12_426.tif (.pcx) on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.3 EXPERIMENT WITH THE UP-COUNTING MODULO-6 COUNTER

4.3.1 Follow the actions of sections 4.2.1 through 4.2.3 but for ones concerning the signal Q_D , which does not exist in the modulo-6 counter circuit; replace Q_D by Q_C .

4.3.2 Adjust the frequency of the Agilent 33120A function generator to 1.25 MHz. Set the triggering mode of the Agilent 54645D to the combination 101 on channels D0 through D2. Hit the key Single on the Agilent 54645D. Adjust the display so that the combination 101 of the counter's output signals is positioned at the left side of the screen, and that the whole screen shows ten percent more than two periods of the signal at Q_C .

4.3.3 Observe the captured modulo-6 up-counter's output waveforms. Compare these waveforms with the contents of Table T2.2-1 of the Assignment #11 Report.

4.3.4 Save the Screen Image of the correct waveforms of channels D0 through D3 to a file named l12_434.tif (.pcx) on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.4 TRANSFER OF CAPTURED WAVEFORMS.

Transfer (ftp) the files l12_*.tif from the Dell GxaEM computer system to your personal College of Engineering computer account.

5. Lab Report

To be considered complete, the lab report must contain the following,

1. Cover sheet - Lab style, filled out,
2. The state transition tables prepared under 2.1 through 2.2 of the Lab Assignment #11.
3. The logic circuit diagrams prepared under 2.1 through 2.2 of the Lab Assignment #11.
4. A copy of the Signal to pin assignment table of the Lab Assignment #12.
5. The waveforms captured in experiments 4.2 through 4.3.
6. Answers to all questions asked in conjunction with experiments 4.2 through 4.3.
7. A report on items not already included under 1. through 6. above, which includes:
   - a discussion of the insights gained through the conducted experiments,
   - textual description and graphical/ tabular illustration of the design procedure(s),
   - description of implemented testing procedures,
   - conclusions reached as a result of performing the lab experiment,
   - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.